SPECIFICATION

Please amend paragraph [0001] of the specification as follows:

[0001] The present document contains material related to the material of copending, cofiled, ~~U.S. patent applications Attorney Docket Number 100111221-1, entitled System And Method For Determining Wire Capacitance For A VLSI Circuit; Attorney Docket Number 100111227-1, entitled System And Method For Determining Applicable Configuration Information For Use In Analysis Of A Computer Aided Design; Attorney Docket Number 100111230-1, entitled Systems And Methods For Determining Activity Factors Of A Circuit Design; Attorney Docket Number 100111232-1, entitled System And Method For Determining A Highest Level Signal Name In A Hierarchical VLSI Design; Attorney Docket Number 100111233-1, entitled System and Method For Determining Connectivity Of Nets In A Hierarchical Circuit Design; Attorney Docket Number 100111234-1, entitled System And Method Analyzing Design Elements In Computer Aided Design Tools; Attorney Docket Number 100111235-1, entitled System And Method For Determining Unmatched Design Elements In A Computer Automated Design; Attorney Docket Number 100111236-1, entitled Computer Aided Design Systems And Methods With Reduced Memory Utilization; Attorney Docket Number 100111238-1, entitled System And Method For Iteratively Traversing A Hierarchical Circuit Design; Attorney Docket Number 100111257-1, entitled Systems And Methods For Establishing Data Model Consistency Of Computer Aided Design Tools; Attorney Docket Number 100111259-1, entitled Systems And Methods For Identifying Data Sources Associated With A Circuit Design, and Attorney Docket Number 100111260-1, entitled Systems And Methods For Performing Circuit Analysis On A Circuit Design,~~ U.S. Patent Application Number 10/647,597, entitled System And Method For Determining Wire Capacitance For A VLSI Circuit; U.S. Patent Application Number 10/647,595, entitled System And Method For Determining Applicable Configuration Information For Use In Analysis Of A Computer Aided Design; U.S. Patent Application Number 10/647,594, entitled Systems And Methods For Determining Activity Factors Of A Circuit Design; U.S. Patent Application Number 10/647,768, entitled System And Method For

Determining A Highest Level Signal Name In A Hierarchical VLSI Design; U.S. Patent Application Number 10/647,606, entitled System And Method For Determining Connectivity Of Nets In A Hierarchical Circuit Design; U.S. Patent Application Number 10/647,596, entitled System And Method Analyzing Design Elements In Computer Aided Design Tools; U.S. Patent Application Number 10/647,608, entitled System And Method For Determining Unmatched Design Elements In A Computer-Automated Design; U.S. Patent Application Number 10/647,598, entitled Computer Aided Design Systems And Methods With Reduced Memory Utilization; U.S. Patent Application Number 10/647,688, entitled System And Method For Iteratively Traversing A Hierarchical Circuit Design; U.S. Patent Application Number 10/647,769, entitled Systems And Methods For Establishing Data Model Consistency Of Computer Aided Design Tools; U.S. Patent Application Number 10/647,607, entitled Systems And Methods For Identifying Data Sources Associated With A Circuit Design, and U.S. Patent Application Number 10/647,605, entitled Systems And Methods For Performing Circuit Analysis On A Circuit Design, the disclosures of which are hereby incorporated herein by reference.

Please amend paragraph [0028] of the specification as follows:

[0028] An exemplary circuit design 116' with four design blocks A-D is now discussed in connection with FIG. 4, FIG. 5 and FIG. 6. FIG. 7 then illustrates one process for generating fast analysis information of circuit design 116'; and FIG. 8 illustrates one process for utilizing the fast analysis information during detailed analysis of circuit design 116'. More particularly, the four design blocks A, B, C and D of FIG. 4 illustrate a hierarchical circuit design 116', which may for example represent circuit design 116 of FIG. 3. Design block A includes design blocks B and C; design block B includes design block C; and design block C twice includes design block D of FIG. 1. Design block D does not incorporate other design blocks. Design elements are not shown within design blocks A, B, C and D for clarity of illustration. A design engineer defines design blocks A-D prior to instantiation within circuit design 116'.